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(54) Tuner for digital receiver with multiple input and multiple output channels

(57) The present invention teaches a compact and highly integrated multiple-channel digital tuner and receiver architecture, suitable for widespread field deployment, wherein each receiver demodulator channel may be remotely, automatically, dynamically, and economically configured for a particular cable, carrier frequency, and signaling baud-rate, from an option universe that includes a plurality of input cables, a plurality of carrier frequencies, and a plurality of available baud-rates. A multiple coax input, multiple channel output, digital tuner is partitioned into a multiple coax input digitizer portion (900) and a multiple channel output front-end portion (6000). The digitizer portion consists of N digitizers and accepts input signals from N coax cables (1800-1...1800-N) and digitizes them with respective A/D converters (930-1...930-N). The front-end portion (6000) consists of M front-ends and provides M channel outputs suitable for subsequent processing by M respective digital demodulators. In a first clock domain (1100), a fixed predetermined A/D sampling rate is chosen to provide oversampling of the inputs by a common integer multiple of all the symbol rates of interest. A plurality of other clock domains (1200,1300-1) operate at selectable sub-multiples of the first domain (1100) as required to deliver a constant number of symbol samples at the output of each front-end. At the input to each of the M front-ends is a respective input selector (2000-1...2000-M) coupled to each of the N streams of digitized input data followed by a digital signal scaler (3000-1...3000-M) that dynamically scales the selected incoming stream of digitized input data as a function of the signal power of the channel's associated carrier.

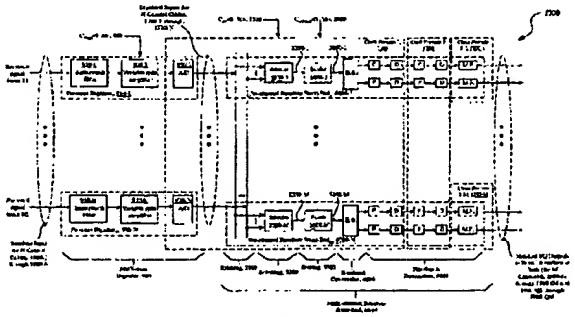

Fig. 2

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Description

BACKGROUND

[0001] Hybrid Fiber Coax (HFC) networks have been used for some time to implement or upgrade metropolitan area cable television systems. In a recent improvement to HFC networks, mini-Fiber-Nodes (mFNs) have been employed to extend fiber closer to subscribers, each mFN providing bidirectional fiber-based services (including Internet access via cable modem) for multiple-tens of subscribers. mFNs are intended to be compact units deployed in the field, generally in aerial-wire or utility-pole-mount configurations, and include at least one "upstream" receiver. An upstream receiver is a receiver in the return direction, that is, in the direction from the subscriber to the cable head end. Generally multiple coaxial (coax) cables, each carrying upstream signals corresponding to a different group of subscribers, may terminate at the mFN for subsequent upstream transmission via fiber.

[0002] Each of these coax cables generally has a wide spectrum (up to 1GHz) including a multiplex of upstream carriers located in the 5-42 MHz range. In accordance with the DOCSIS industry standard, each upstream carrier may have any symbol rate from 5 possible values (160 kBaud, 320 kBaud, 640 kBaud, 1280 kBaud, 2560 kBaud) with a modulation format of either QPSK or 16-QAM. In addition, each upstream carrier has a power spectrum density variation, with respect to a nominal value, of ±6 dB. In a worst-case scenario for the upstream receiver, the 5-42MHz band may be filled with (up to 11) undesired carriers operating with the maximum baud rate (2560 kBaud) and a desired carrier may have the smallest value 160 kBaud. Furthermore, there may be up to a 12 dB difference in power spectrum density between the desired carrier and the others.

[0003] A digital receiver may be partitioned into a tuner and digital demodulator portions. The tuner accepts one or more broadband analog inputs having a variety of desired and undesired signals. The tuner's purpose is to isolate the desired signals and provide baseband-translated digitized equivalents for subsequent processing in the demodulator. Because quadrature modulation is common, the outputs are often provided in quadrature. The stage(s) where frequency translation is performed is (are) generally referred to as the receiver front-end. The stages where digitization is performed may be referred to as the A/D (ADC, analog to digital converter, or digitizer). The stages before and after the A/D are necessarily analog and digital, respectively.

[0004] A traditional tuner for an upstream digital receiver is shown in Fig. 1. A first IF (intermediate frequency) conversion combined with a SAW (surface acoustic wave) filter is used for isolating the desired carrier and suppressing any and all undesired carriers. Next, down-conversion is done in the analog domain by in-phase splitting the isolated carrier and mixing with 2 analog LOs (local oscillators). The analog LOs are provided in quadrature at the expected channel spacing. Each of the resulting quadrature signals from the mixers is then coarse anti-alias filtered in the analog domain and sampled with respective A/Ds. Matched filtering after the A/Ds is subsequently performed in the digital domain. The quadrature output signal pair of the matched filter may then be provided to the demodulator of the desired carrier/channel.

[0005] There are a number of significant costs associated with each required stage of any digital receiver tuner. Costs are minimized by keeping stages as simple as possible and as few in number as necessary. Another stage cost is associated with the bit-width of the digital stages. Each additional bit in width incrementally increases the cost, size, and complexity of the associated receiver. Since the dynamic range of the signals being processed necessitates a proportional bit-width, the dynamic range should be minimized consistent with maintaining good performance. Because A/Ds are often the most complex and expensive sub-systems in the tuner, the number of required A/Ds is a key implementation consideration. In addition, each A/D has an associated clock sub-system (not shown in Fig. 1 but known to practitioners of the art) that must be configured appropriately for the carrier being digitized. The number and extent of required clock sub-systems is thus also an important implementation consideration.

[0006] Traditional digital receiver approaches have required the entirety of the above-described tuner per desired carrier/channel. In the mFN augmented HFC systems discussed above, because of the associated expense, bulk, and complexity of the traditional tuners, it has not been considered practical in widespread deployment to demodulate upstream signals locally at the mFN. Accordingly, the entire spectrum of each coax has been indiscriminately sent upstream over fiber via either analog or digital techniques for remote reconstruction and demodulation at the cable head end (or intermediate upstream location). Accordingly, when multiple coaxial cables terminate into the mFN, ether multiple expensive fibers are required or expensive WDM techniques have been used to multiplex the multiple coax spectra onto respective "lambda" wavelengths of a single fiber. In these approaches, the ultimately demodulated upstream information content is a small fraction of the transmitted upstream bandwidth.

[0007] In applications (such as upstream cable modem traffic) where there are multiple desired channels on each of generally multiple input coaxial cables, the use of traditional digital receivers (requiring one tuner per desired carrier/channel) results in a confusing proliferation of associated splitters, connectors, and couplers. Provisioning (establishing the operating configuration of) a particular upstream subscriber signal (out of many)

over a particular upstream channel (again out of many) generally necessitates error-prone manual configuration of multiple coaxial cables, splitters, connectors, and couplers. This hardware also introduces new noise and signal losses. Provisioning additionally involves configuration of the receiver to accommodate the carrier frequency and baud-rate of the transmitted signal. To change the carrier frequency dynamically in the traditional digital receiver requires a very agile and very costly local oscillator. Less expensive, less agile, local oscillators generally necessitate error-prone manual configuration of component modules or component settings.

[0008] It is thus seen that there are many shortcomings to the traditional tuner approaches to multiple input, multiple output channel, digital receivers. What is needed is an optimized tuner for such receivers that is efficient, cost sensitive, flexible, and minimizes noise and signal loss. What is needed is a multiple input, multiple output channel, digital receiver tuner that reduces the number of signal processing stages, the stage bit-widths, the number of A/Ds, and the number and extent of clock sub-systems compared with traditional approaches. What is further needed is a compact and efficient multiple input, multiple output channel, digital receiver that performs local demodulation and is suitable for widespread field deployment in distributed communication systems and networks.

SUMMARY

[0009] The present invention teaches a compact and highly integrated multiple-channel digital tuner and receiver architecture, suitable for widespread field deployment, wherein each receiver demodulator channel may be remotely, automatically, dynamically, and economically configured for a particular cable, carrier frequency, and signaling baud-rate, from an option universe that includes a plurality of input cables, a plurality of carrier frequencies, and a plurality of available baud-rates. The invention thus provides substantial additional flexibility and cost savings over conventional multiple-channel receiver approaches where equivalent configuration capability would require prohibitively expensive specialized components or costly manual operations that cannot be implemented automatically. Tuners and digital receivers implemented in accordance with the present invention also minimize the number of required A/Ds, number and extent of clock sub-systems, bit-width of digital processing stages, and overall complexity. The architecture has broad generic applicability, but offers particular advantages in multiple (coax) input, multiple channel output, digital receivers. In a series of illustrative embodiments, the teachings of the invention are applied to an upstream digital receiver sub-system for use in the mFNs of an HFC network.

[0010] In accordance with a first aspect of the present invention, an illustrated multiple coax input, multiple channel output, digital tuner embodiment is partitioned into a multiple coax input digitizer portion and a multiple channel output front-end portion. The digitizer portion consists of a number (N) of digitizers and accepts input signals from N coax cables and digitizes them with respective A/D (Analog-to-Digital) converters. This creates N streams of digitized input data, respectively corresponding to each coax cable. The front-end portion consists an independent number (M) of front-ends and provides M channel outputs, which are streams of baseband-translated digital words suitable for subsequent processing by M respective demodulators. At the input to each of the M front-ends is a respective input selector coupled to each of the N streams of digitized input data. Thus, each of the M front-ends is selectively configurable to process digitized input data corresponding to any of the N coax cables. Collectively, the input selectors comprise a selector bank. The selector bank is a compact and efficient implementation that elegantly operates in the digital domain to provide functionality previously performed in the analog domain by bulky analog splitters that are problematic and costly to provision.

[0011] In accordance with a second aspect of the present invention, a variable-gain amplifier is situated before the A/D converter used to digitize the input signals for each of the N coax inputs, and a digital signal scaler is situated at the input of each of the M front-ends. The variable-gain amplifier that precedes the A/D converter operates on the entire carrier multiplex that is present on the associated coax. The amplifier gain is set as a function of the entire carrier multiplex present on the coax and not by any particular carrier. Each digital signal scaler is dedicated to a respective front-end channel and therefore has a particular respective carrier of interest. The scaler dynamically scales (shifts right or left by one or more bits) the incoming stream of digitized input data as a function of the signal power of the respective carrier in order to minimize variations in the peak magnitude of the signals processed. The scaler thus manages the dynamic range such that the digital-word bit-width of the digital front-end and subsequent demodulator stages can be minimized consistent with good performance, substantially reducing the complexity and cost of the digital receiver.

[0012] In accordance with a third aspect of the present invention, a particular clocking combination is used within the digital receiver tuner. A fixed predetermined A/D sampling rate is chosen to provide oversampling of the inputs by a common integer multiple of all the symbol rates of interest. Each oversampled input stream is digitally down-converted to baseband and processed in three sample-frequency domains. The first domain includes in common the A/Ds of the N digitizers, the baseband converters and first decimators of the M front-ends, and operates at the fixed A/D sample rate. In an optional but preferred embodiment, a second domain, including a second decimator,

operates at a fixed sub-multiple of the first domain. Additional clock domains exist, including a plurality operating at selectable sub-multiples of the first domain (or second domain, if any) as required to deliver a constant number of symbol samples to each matched filter of the respective front-ends. This clocking approach enables producing matched front-end outputs using only simple filters and decimation, eliminates the need for interpolation stages, maximizes commonality of function, and provides reduced complexity and costs over previous approaches.

Brief Description of Drawings

[0013] Fig. 1 illustrates a prior art tuner for a digital receiver.

[0014] Fig. 2 illustrates a tuner 1000 for a digital receiver in accordance with the present invention, including a multiple-coax digitizer 900 and a multiple-channel front-end 6000.

[0015] Fig. 3 is a drawing providing additional detail of the splitting 2100 and selecting 2200 function blocks of the tuner 1000 of Fig. 2.

[0016] Figs. 4A-4D are drawings providing conceptual detail of the scaler 3000 of the tuner 1000 of Fig. 2 for four different operating cases. Fig. 4A illustrates the unity gain, no-shift case. Fig. 4B illustrates a shift by one bit in the LSB direction. Fig. 4C illustrates a shift by two bits in the LSB direction. Fig. 4D illustrates a shift by three bits in the LSB direction.

[0017] Fig. 5 illustrates the baseband conversion 4000 and filtering and decimation 5000 function blocks of a single channel in the tuner 1000 of Fig. 2.

[0018] Fig. 6 illustrates preferred chip-boundary partitions for two different illustrative embodiments of the tuner 1000 of Fig. 2

[0019] Figs. 7 and 8A-C illustrate exemplary system-level application of the present invention. Fig. 7 illustrates a mini-Fiber-Node/mini-Cable-Modem-Termination-System (mFN/mini-CMTS) 8000 using a DSP multiple-channel transceiver ASIC 7000, which implements in silicon the multiple-channel receiver front-end 6000 portion of the tuner 1000 of Fig. 2.

[0020] Figs. 8A-C illustrate the routing between a Head End 10100, the Internet 10000, and Customer Premise Equipment (CPE) 8B, in a cable system architecture using the mFN/mini-CMTS 8000 of Fig. 7. Fig. 8A provides particular detail of the routing between the Head End 10100, Regional Packet Network 10150, mFN/mini-CMTS 8000, and CPE 8B. Fig. 8B provides particular detail of the CPE 8B. Fig. 8C provides particular detail of the routing between the Head End 10100 and the Internet 10000.

Detailed Description

[0021] Fig. 2 illustrates a multiple coax input, multiple channel output, digital tuner 1000 for a digital receiver in accordance with the present invention, including a multiple-coax digitizer portion 900 and a multiple-channel front-end portion 6000. The digitizer portion 900 consists of N Per-coax Digitizers 900-1 through 900-N, accepts input signals 1800-1 through 1800-N from N coax cables, digitizes them with respective A/D converters 930-1 through 930-N, and delivers to the front-end digitized signals 1700-1 through 1700-N. A Butterworth filter 910 and variable-gain amplifier 920 precedes each A/D converter. While a Butterworth characteristic is used in the illustrative embodiment, this choice is not critical and other low-pass filters may also be used. The variable-gain amplifier 920 is set by control 950 as a function of the entire carrier multiplex present on the amplifier's associated coax input. The front-end portion 6000 consists of M Per-channel Receiver Front-ends 6000-1 through 6000-M. The functions performed by front-end 6000 include splitting 2100, selecting 2200, scaling 3000, baseband conversion 4000, and filtering and decimation 5000. Front-end 6000 provides M channel output quadrature pairs 1900-I1 through 1900-IM and 1900-Q1 through 1900-QM suitable for subsequent processing by M respective digital demodulators. Digitized signals 1700-1 through 1700-N are distributed to the individual selectors via splitting 2100. In accordance with control 2500, each selector 2000 couples a selected one of the digitized inputs to the subsequent stages of the front-end. In accordance with control 3500, the digital signal scaler 3000 dynamically scales the selected incoming stream as a function of the signal power of the channel's associated carrier.

[0022] Clock domain 1100 includes in common the A/Ds 930-1 through 930-N of the N digitizers 900-1 through 900-N and a first sub-portion of the M front-ends, and operates at a fixed A/D sample rate chosen in accordance with a specific criteria to be discussed below. A second clock domain 1200, including a second sub-portion of the M front-ends, facilitates implementation and operates at a fixed sub-multiple of the first domain. Additional clock domains exist, including a plurality 1300-1 through 1300-M operating at selectable sub-multiples of the first domain as required to deliver a constant number of symbol samples to outputs of the front-end.

Digital Splitter

[0023] Fig. 3 is a drawing providing additional detail of the splitting 2100 and selecting 2200 function blocks of the tuner 1000 of Fig. 2. Digitized signals 1700-1 through 1700-N are distributed to the individual selectors via splitting 2100, shown here as simple distribution interconnect. Practitioners will understand that additional well-known considerations such as buffering and attention to interconnect impedances and parasitics may be required based on implementation specifics. In accordance with control 2500, each selector 2000 couples a selected one of the digitized inputs to the subsequent stages of the front-end. Practitioners will understand that the selectors may use either encoded or uncoded controls and that the number of control bits will vary based on this choice and the number of inputs being selected. The outputs 2250-1 through 2250-M are provided to subsequent stages of the front-end.

[0024] Collectively, the input selectors comprise a selector bank. Via the selector bank, each demodulator channel is selectively configurable to process digitized input data corresponding to any of the coax cables. The selector bank elegantly operates in the digital domain to provide functionality previously performed in the analog domain by manual configuration of splitters, couplers, cables, and connectors that are problematic and costly to provision.

[0025] Thus in accordance with the present invention, a modulated input signal corresponding to a particular subscriber, and on a particular one of the coaxial cables, can be routed (sent) to any particular one of the plurality of demodulator channels. In the illustrative embodiment, the routing configuration is established during provisioning of the upstream channel for each subscriber, the input selector for each demodulator channel being controlled by digital commands transmitted from the head end. Provisioning the upstream channel in this way reduces or eliminates the manual configuration of connectors and couplers; reduces additional sources of noise and signal losses; speeds setup; reduces costs; and increases flexibility. More generally, the input selectors could be reconfigured dynamically, in response to predefined criteria, to provide fault tolerance or minimization of transient interference.

Dynamic Range And Signal Power Management

[0026] The inventors discovered that control over signal power in digital receiver front-ends is optimally managed through a cooperative combination of variable-gain amplifiers in the analog domain and digital signal scalers in the digital domain. More specifically, a variable-gain amplifier is situated before the A/D converter used to digitize the input signals for each coax, and a digital signal scaler is situated at the input of each front-end. (In accordance with the discussion above, the scaler is placed after any selector function).

[0027] The variable-gain amplifier that precedes the A/D converter operates on the entire carrier multiplex that is present on the associated coax. Recall that the output of the A/D converter may be supplied to multiple demodulator channels, each typically having a respectively unique carrier of interest. The gain of this amplifier is considered appropriately set when the adjusted input to the A/D is such that the digitized output generally spans the dynamic range of the A/D without significant saturation. The amplifier gain is thereby set as a function of the entire carrier multiplex present on the coax and not by any particular carrier. In a particular illustrative embodiment the A/D provides a 12-bit 2's complement output. There is only 11-bits of usable precision however, and the original LSB from the A/D is ignored. The front-end subsequently operates on 11-bit 2's complement digital words.

[0028] In an illustrative tuner embodiment compatible with the DOCSIS industry standard, the power spectral density has a dynamic range of 12 dB. The modulated carrier bandwidth dynamic range, which is proportional to a maximum-to-minimum symbol rate ratio of 16, also is 12 dB. Since the product of the power spectral density and the bandwidth gives received signal power for a selected carrier, the received signal power has a 24 dB dynamic range for a selected carrier in this application. Thus, a front-end designed for this application should have 24dB of headroom.

[0029] Unlike traditional approaches, the 24 dB of required dynamic range headroom is accomplished through use of the digital scaler in accordance with the present invention, and without additional bits over that required by the minimum signal case. More specifically, the digital signal scaler reduces the complexity and the cost of the front-end by limiting the dynamic range to the minimum necessary, while providing good performance.

[0030] Each digital signal scaler is dedicated to a respective front-end channel and therefore has a particular respective carrier of interest. The scaler dynamically scales the incoming stream of digitized input data (by selective shift toward the LSB of zero to three bits) as a function of the received nominal signal power of the respective carrier. The scaler is operated to maintain essentially the same peak signal magnitude (having 3-dB of headroom) at the input to the next stage of the rest of the front-end (the broadband conversion in the illustrative embodiment). As signals increase in amplitude, the scaler selectively shifts by a proportionally greater numbers of bits, providing increasing attenuation.

[0031] Figs. 4A through 4D are conceptual drawings of various shift configurations selected by control 3500. In a preferred embodiment, the scaler is implemented using AND-OR gating, but practitioners will understand that such

shifting functions may be readily implemented via a variety of other techniques. Fig. 4A illustrates the unity gain, no-shift case, corresponding to small amplitude signals. Fig. 4B illustrates a shift by one bit in the LSB direction, corresponding to division by 2 (attenuation to ½ of the input magnitude). Fig. 4C illustrates a shift by two bits in the LSB direction, corresponding to division by 4 (attenuation to ¼ of the input magnitude). Fig. 4D illustrates a shift by three bits in the LSB direction, corresponding to a division by 8 (attenuation to 1/8 of the input magnitude).

Front-End Stages

[0032] Within the previously discussed digitizer portion of the tuner 1000 of Fig. 2, the received signal is oversampled by an A/D operating at

$$F_{sampling}=102.4 \text{ MHz}.$$

[0033] The extent of oversampling and the specific frequency chosen are in accordance with criteria discussed in the next section below. Subsequent to the digitizer, the oversampled input is selected and scaled as discussed previously above. With reference now made to Fig. 5, the oversampled, selected, scaled, input stream 3050 is subsequently digitally down-converted within baseband conversion 4000 into baseband orthogonal component streams (4150-I and 4150-Q). This is done by parallel multiplications 4100-I and 4100-Q of the digitized signal 3050 with the quadrature local oscillator signals 4125-I and 4125-Q, represented by the complex exponential

$$e^{2j\pi kF_I T_{sampling}}$$

where F_I is the nominal carrier frequency and

$$T_{sampling}=1/F_{sampling}.$$

[0034] Each of the quadrature baseband digital streams (4150-I and 4150-Q) is then parallel processed by the Filtering and Decimation functions 5000 in respective but otherwise identically implemented filter and decimation pipelines. For each pipeline, 2 low-pass FIR (finite impulse response) filters (5100 and 5300), 2 decimators (5200 and 5400), and a matched filter 5600 are provided. The number and arrangement of the filters and decimators are chosen for reasons discussed in the next section below. However, the overall purpose of the decimators is to reduce the number of samples to a constant 4 samples per symbol period, independent of baud rate.

[0035] The purpose of the low-pass filters is to reject the image frequencies resulting from the baseband conversion and any adjacent undesired carriers. In the illustrated preferred embodiment, each low-pass filter is implemented as a cascaded integrator comb (CIC) filter. The impulse response of the CIC filter is given by

$$\left(\sum_{i=0}^{N} z^{-i}\right)^{D},$$

where N corresponds to the decimation factor and D to the number of cascaded integrators. With D=4, better than 50dB of out-of-band rejection is obtained, which is sufficient for the applications of the illustrated embodiments.

[0036] In a purely theoretical receiver, the matched filter of the front-end should have an impulse response exactly matched to that of the theoretical transmit filter. Both may be chosen to be identical square-root raised-cosine filters, so that their cascade provides a raised cosine Nyquist filter. Such a filter guarantees zero-ISI (zero-intersymbol interference) while minimizing the noise at the detector input. In actual implementations, the CIC filters have a known non-ideal response (it is not flat) in the pass band that can be compensated for by appropriate adjustments to the response of the matched filter. Thus in the illustrated preferred embodiment, the matched filter implements an FIR whose coefficients are those of a squared-root raised cosine filter compensated for the CIC filters attenuation.

Multi-Symbol Rate Demodulation Using a Fixed Sampling Rate

[0037] In an illustrative embodiment compatible with the DOCSIS standard, the sampling frequency is chosen to be a fixed integer multiple of all symbol rates in accordance with another aspect of the present invention. Recall that in the DOCSIS standard, each of the input coax cables may have a multiplex of carriers located in the 5-42 MHz range and that each carrier may have any symbol rate from 5 possible values (160 kBaud, 320 kBaud, 640 kBaud, 1280 kBaud, 2560 kBaud).

[0038] In particular, the sampling frequency is chosen to be an integer multiple of 4 times the symbol rates, so that 4 samples per symbol interval can be fed to the matched filter after simple decimation. Furthermore, since the

multiplex on each cable has a spectrum which spans the 5-42 MHz frequency range, the sampling frequency must be higher than 84 MHz (twice the maximum frequency). All these conditions are satisfied by the previously cited sampling frequency of 102.4 MHz. This frequency corresponds to an over-sampling factor equal to 10, 20, 40, 80, 160 when the baud rate is 2560 kBaud, 1280 kBaud, 640 kBaud, 320 kBaud, 160 kBaud, respectively.

[0039] A number of options are possible in implementing the tuner's decimation from the A/D sample rate to the 4 samples per symbol interval rate. For the illustrative application, the tuner decimates by a selected total factor of 10, 20, 40, 80, or 160. It is possible to achieve these rate changes in a single stage with a configurable decimation (rate change) factor, through multiple stages of which each has a configurable decimation factor, or through multiple stages of which some have a fixed decimation factor and others have a configurable decimation factor. In multiple stage decimation approaches, the particular rate change stage partitioning (or ordering) used to accomplish the total required rate change is not crucial to the overall operation. While a particular partitioning and ordering is used in the illustrative embodiment, practitioners will realize that other partitioning and orderings are possible within the scope of the present invention.

[0040] In the embodiment illustrated in both Fig. 2 and Fig. 5, the tuner is partitioned into multiple sample-frequency clock domains. The first domain 1100 operates at the fixed A/D sample rate and includes in common the A/Ds 930 of the N digitizers 900, the baseband converters 4100, and the first decimators 5200 of the M front-ends 6000. Additional clock domains 1300 exist, including a plurality operating at selectable sub-multiples of the first domain (or second domain, if any, as discussed below) as required to deliver a constant number of symbol samples (4 in the illustrated embodiment) to each matched filter of the respective front-ends.

[0041] In an optional but preferred embodiment, a second domain 1200, including a second decimator 5400, operates at a fixed sub-multiple of the first domain. Using this preferred approach, the decimation is done in two separate steps. The first decimator 5200 operates with a constant "rate change" ratio equal to 10 (i.e., it keeps one of every 10 samples). The second decimator 5400 has a configurable rate change ratio whose value is selectable between 1 and 16, depending on the symbol rate. The dependence of the rate change ratio on the symbol rate as it is shown in Table 1.

Table 1.

Rate Change Ratio for each Symbol Rate.			
Symbol rate (kBaud)	Total rate change ratio	1st stage rate change ratio	2nd stage rate change ratio
160	160	10	16
320	80	10	8
640	40	10	4
1280	20	10	2
2560	10	10	1

[0042] In summary, in the illustrated embodiment only the first stages of the front-end operate at the sampling frequency of 102.4 MHz, while subsequent stages operate at 10.24 MHz, and the final stages (including the matched filter) operate at 4 times the symbol rate.

[0043] The clocking approach taught by the present invention enables producing matched front-end outputs using only simple filters and decimation, eliminates the need for interpolation stages, maximizes commonality of function, and provides reduced complexity and costs over previous approaches.

System-Level Implementation

[0044] Fig. 6 illustrates preferred chip-boundary partitions for two different illustrative embodiments of the tuner 1000 of Fig. 2. It is desirable to implement as much as possible of the tuner 1000 on a single integrated circuit, consistent with sound engineering and business practice. System partition 1050 corresponds to a preferred illustrative implementation, wherein all stages of the tuner following variable gain amplifier 920 are integrated on a single integrated circuit, generally with other functions. However, due to the size and complexity of the A/Ds, the more conservative system partition 1050 may be chosen.

[0045] Figs. 7 and 8A-C further illustrate an exemplary system-level application of the present invention. Fig. 7 illustrates a mini-Fiber-Node/mini-Cable-Modem-Termination-System (mFN/mini-CMTS) 8000. The mini-CMTS 9000 implements a multi-channel digital receiver that employs a tuner 1000 in accordance with the present invention.

Consistent with the system partition 1050 of Fig. 6., the front-end portion 6000 of the tuner is implemented on the DSP multi-channel transceiver ASIC 7000. Also implemented on the ASIC is the multi-channel demodulator portion of the digital receiver as well as the all-digital portions of a multi-channel digital transmitter. The tuner 1000 accepts multiple coax inputs 1800, delivers digitized equivalent streams 1700 from the output of digitizer portion 900, and delivers baseband converted and isolated quadrature digitized signals 1900, suitable for demodulation. The realization locally within the mFN of the CMTS functions, in general and the demodulator functions in particular, is made practical for widespread deployment by the teachings of the present invention.

[0046] Fig. 8A shows the relationship between the mFN and subscribers (indicated by homes having Customer Premise Equipment, CPE) and between the mFN and the cable system head end 10100. Each mFN is coupled to up to 50 to 70 homes (50-70 Households Passed, HHP). Each mFN is coupled to the head end via a regional packet network 10150. This packet network is usually implemented as a packet fiber overlay for a downstream legacy analog HFC distribution. Fig. 8B provides detail of the CPE, which generally includes a television, the cable "set-top" box, and a cable modem for coupling the subscriber's personal computer to the network. In some systems, the CPE may additionally include an interface to a subscriber telephone.

[0047] Fig. 8C shows the Head End 10100 as a component within the Internet 10000. As indicated in the legend, many subcomponents are part of this network. In this conceptual drawing, multiple backbone networks 10050-1 through 10050-N, generally operated by different long-haul communications companies, are interconnected via Peering Point 10100-1 (and other peering points not shown). Dial-up access provider 10500, Server Farm 10400, corporate network 10300, and cable system head end 10100, contract for access to the various backbone networks. Corporate end-user 10390 has network access via the associated corporate network 10300. Private end-user 10550 has access via dial-up connection 10540. Thus in the illustrated embodiments provided, cable subscribers (as indicated by homes illustrated in Fig. 8A) provide or gain access to content, services, e-mail, and other Internet resources, via a path that includes the multiple input, multiple channel output, digital tuner of the present invention.

Conclusion

[0048] Although the present invention has been described using particular illustrative embodiments, it will be understood that many variations in construction, arrangement and use are possible consistent with the teachings and within the scope of the invention. For example, bit-widths, clock speeds, and the type of technology used may generally be varied in each component block of the invention. Also, unless specifically stated to the contrary, the value ranges specified, the maximum and minimum values used, are merely those of the illustrative or preferred embodiments and should not be construed as limitations of the invention. Specifically, other embodiments may use different clock multiples or sub-multiples, different frequency bands, different modulation schemes, and different numbers of inputs and output channels. Functionally equivalent techniques known to those skilled in the art may be employed instead of those illustrated to implement various components or sub-systems. For example, the selector and scaler functions may be implemented using pass-gates or tri-state buffers and not just via the preferred AND-OR gating. All such variations in design comprise insubstantial changes over the teachings conveyed by the illustrative embodiments. The names given to interconnect and logic are illustrative, and should not be construed as limiting the invention. It is also understood that the invention has broad applicability to other communications and network applications, and is not limited to the particular application or industry of the illustrated embodiments. The present invention is thus to be construed as including all possible modifications and variations encompassed within the scope of the appended claims.

Claims

1. A method of operating a digital tuner, comprising:

   digitizing a first number of input signals to create respective streams of digitized input data;

   providing a second number of per-channel front-ends for performing baseband translation and filtering in the digital domain and providing outputs suitable for subsequent demodulation;

   providing each per-channel front-end with an input selector coupled to each of the streams of digitized input data; and

   configuring each of the per-channel front-ends to process a selected one of the first number of streams of digitized input data.

2. A method of operating a digital tuner, comprising:

providing a first number of A/D converters for digitizing a first number of input signals to create respective streams of digitized input data;

providing each A/D converter with a preceding variable-gain amplifier;

setting the amplifier gain as a function of the entire carrier multiplex present on the input signals;

providing a second number of per-channel front-ends for performing baseband translation and filtering in the digital domain and providing outputs suitable for subsequent demodulation;

providing each per-channel front-end with a respective digital signal scaler coupled to a selected one of the streams of digitized input data;

providing the output of the scaler to the subsequent stages of its respective per-channel front-end; and

for each per-channel front-end, dynamically scaling the selected incoming stream of digitized input data as a function of the signal power of the desired carrier to minimize variations in the peak magnitude of the signals processed.

3. A method of operating a digital tuner, comprising:

providing a first plurality of input signals having a second plurality of symbol rates;

providing a first sampling clock that is a common integer multiple of the second plurality of symbol rates;

digitizing the first plurality of input signals using the first sampling clock to create respective streams of digitized input data;

providing a third plurality of per-channel front-ends, each front-end having a baseband converter, a first decimator, and a matched filter;

operating the baseband converter and the first decimator of each per-channel front-end at the first sampling clock; and

for each per-channel front end, providing a selectively decimated number of samples to each matched filter and operating each matched filter at a selected compatible sampling clock, such that a constant number of symbol samples is output from each matched filter.

4. A digital tuner, comprising:

a first plurality of digitizers operating at a common first sampling rate and providing a first plurality of digitized data streams corresponding to a first plurality of analog inputs;

a second plurality of digital front-ends, each front-end including

selector circuitry for selectable coupling of one of the first plurality of digitized data streams to post-selector processing circuitry of the associated front-end, each selector operating independently of the other selectors,

digital frequency conversion circuitry having a selectable conversion frequency from a predetermined set of conversion frequencies, and

post-conversion circuitry having a selectable decimation factor from a predetermined set of decimation factors, the post-conversion circuitry providing an output suitable for subsequent processing by a

digital demodulator; and

wherein configuration of the tuner may select any arbitrary combination of one of the first plurality of analog inputs, one of the set of conversion frequencies, and one of the set of decimation factors.

5. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished programmatically.

6. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished remotely.

7. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished automatically.

8. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished dynamically.

9. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished without involving a human operator.

10. The digital tuner of claim 4, wherein the common first sampling rate is an integer multiple of each decimation factor of the predetermined set of decimation factors.

11. The digital tuner of claim 4, wherein each decimation factor of the predetermined set of decimation factors is an integer sub-multiple of the common first sampling rate.

12. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as a single stage having a configurable decimation factor selected from a predetermined set.

13. The digital tuner of claim 12, wherein the predetermined set includes decimation factors of 10, 20, 40, 80, and 160.

14. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as multiple stages of which some have a fixed decimation factor and others have a configurable decimation factor.

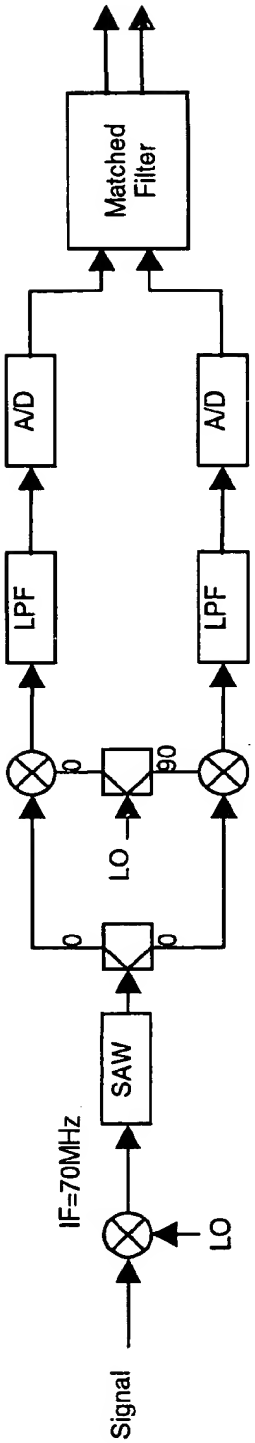
15. The digital tuner of claim 14, wherein the post-conversion circuitry is implemented using a first stage having a fixed decimation factor and a second stage having a configurable decimation factor selected from a predetermined set.

16. The digital tuner of claim 15, wherein the fixed decimation factor is 10.

17. The digital tuner of claim 15, wherein the predetermined set includes decimation factors of 1, 2, 4, 8, and 16.

18. The digital tuner of claim 15, wherein the fixed decimation factor is 10 and the predetermined set includes decimation factors of 1, 2, 4, 8, and 16.

19. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as multiple stages of which each has a configurable decimation factor.



Prior Art
Fig. 1

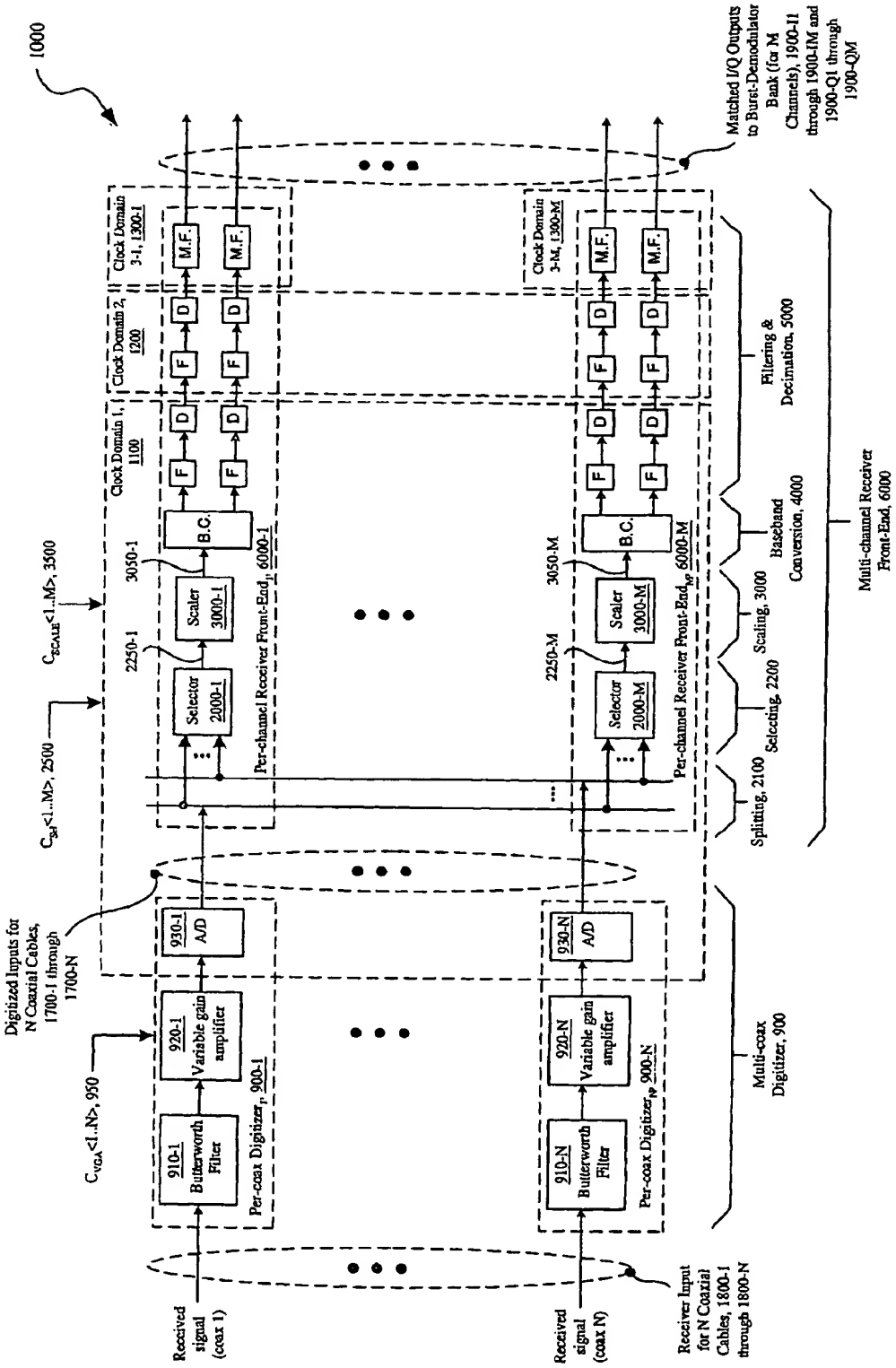

1000
Matched I/Q Outputs to Burst-Demodulator Bank (for M Channels), 1900-11 through 1900-1M and 1900-Q1 through 1900-QM
Clock Domain 3-1, 1300-1
Clock Domain 3-M, 1300-M
Clock Domain 2, 1200
Clock Domain 1, 1100
M.F.
D
F
B.C.
Scaler 3000-1
Scaler 3000-M
Selector 2000-1
Selector 2000-M
3050-1
3050-M
2250-1
2250-M
Per-channel Receiver Front-End, 6000-1
Per-channel Receiver Front-End, 6000-M
Filtering & Decimation, 5000
Baseband Conversion, 4000
Scaling, 3000
Selecting, 2200
Splitting, 2100
Multi-channel Receiver Front-End, 6000
C_{SCALE}<1..M>, 3500
C_{SEL}<1..M>, 2500
C_{VGA}<1..N>, 950
Digitized Inputs for N Coaxial Cables, 1700-1 through 1700-N
930-1 A/D
930-N A/D
920-1 Variable gain amplifier
920-N Variable gain amplifier
910-1 Butterworth Filter
910-N Butterworth Filter
Per-coax Digitizer, 900-1
Per-coax Digitizer, 900-N
Multi-coax Digitizer, 900
Received signal (coax 1)
Received signal (coax N)
Receiver Input for N Coaxial Cables, 1800-1 through 1800-N

Fig. 2

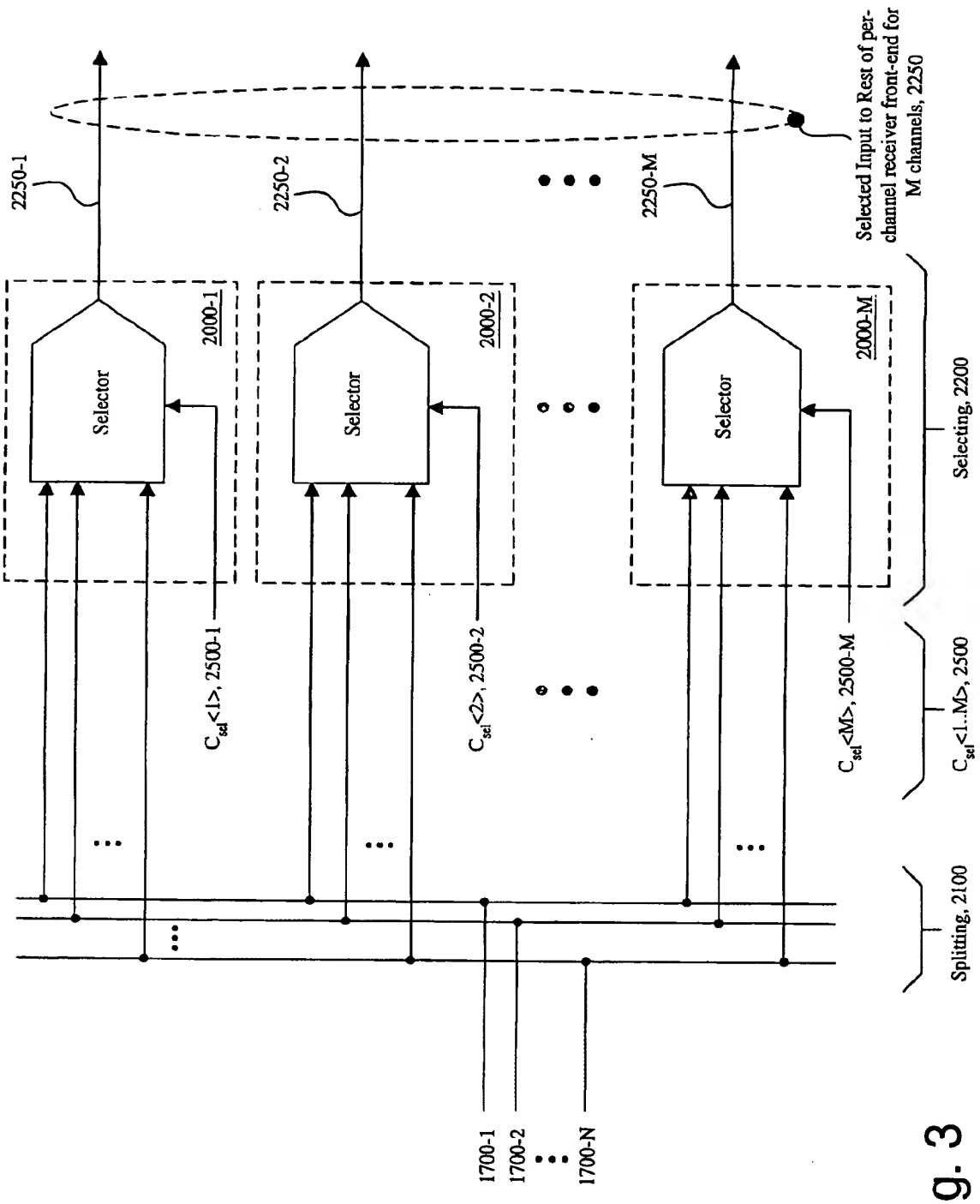

2250-1
2250-2
2250-M
Selected Input to Rest of per-channel receiver front-end for M channels, 2250
Selector
2000-1
2000-2
2000-M
Selecting, 2200
C_{sel}<1>, 2500-1
C_{sel}<2>, 2500-2
C_{sel}<M>, 2500-M
C_{sel}<1..M>, 2500
Splitting, 2100
1700-1
1700-2
1700-N

Fig. 3

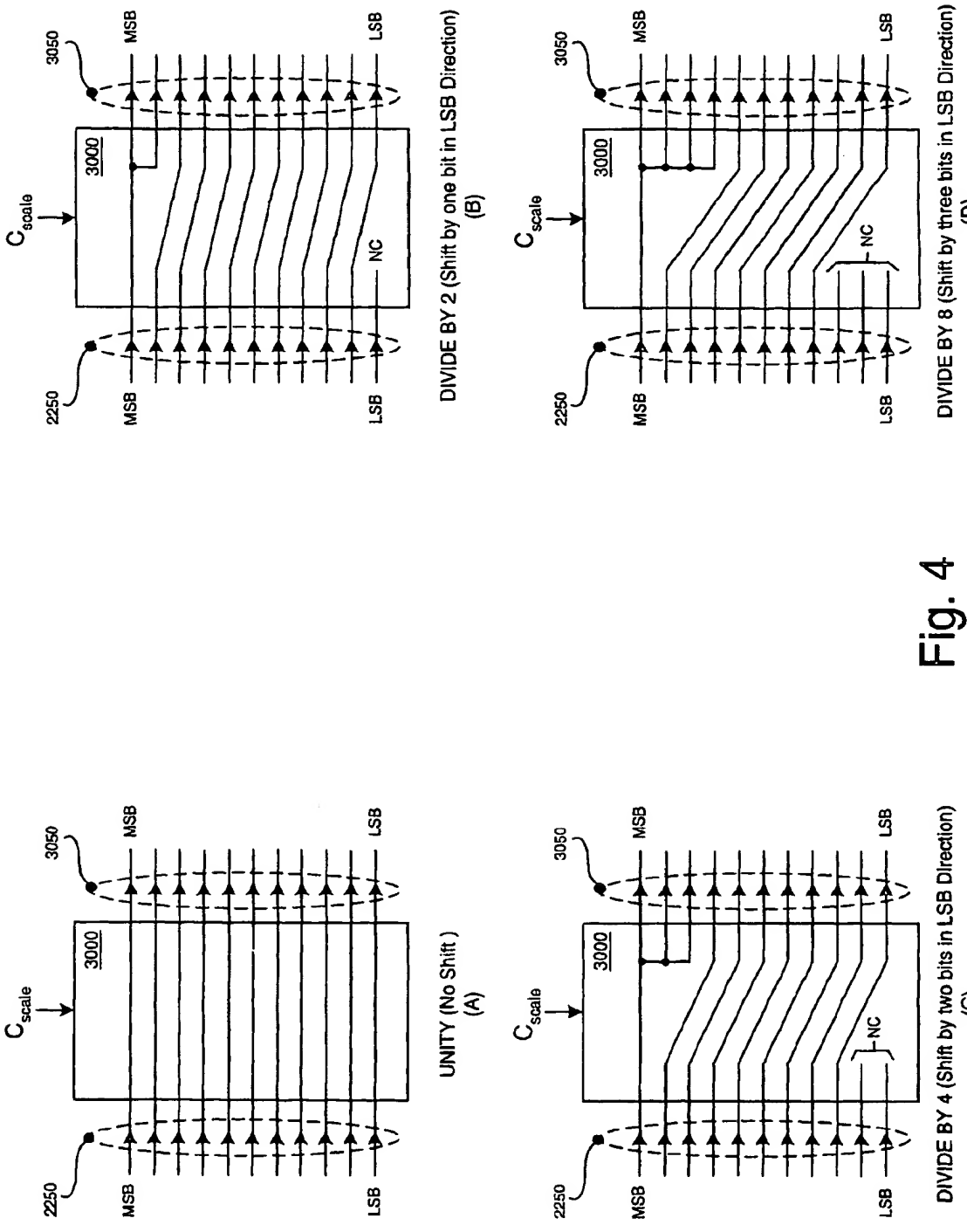

3050
MSB
LSB
3000
C_{scale}
NC
2250
MSB
LSB
DIVIDE BY 2 (Shift by one bit in LSB Direction)
(B)
DIVIDE BY 8 (Shift by three bits in LSB Direction)
(D)
UNITY (No Shift)
(A)
DIVIDE BY 4 (Shift by two bits in LSB Direction)
(C)

Fig. 4

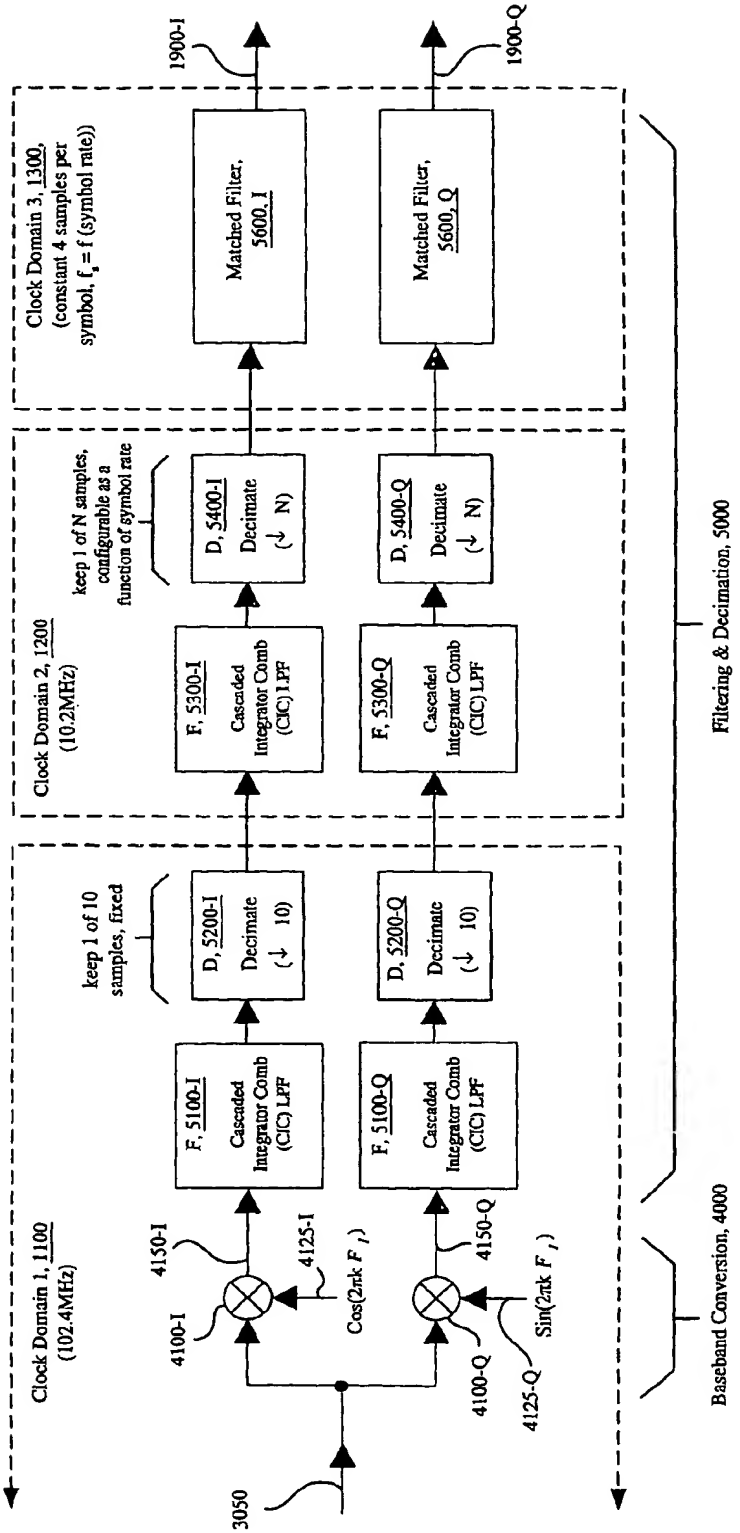

Clock Domain 1, 1100
(102.4MHz)
Clock Domain 2, 1200
(10.2MHz)
Clock Domain 3, 1300,
(constant 4 samples per
symbol, $f_s = f$ (symbol rate))
3050
4100-I
4150-I
4125-I
Cos(2πk F_1)
4100-Q
4150-Q
4125-Q
Sin(2πk F_1)
F, 5100-I
Cascaded Integrator Comb (CIC) LPF
F, 5100-Q
Cascaded Integrator Comb (CIC) LPF
keep 1 of 10 samples, fixed
D, 5200-I
Decimate (↓ 10)
D, 5200-Q
Decimate (↓ 10)
F, 5300-I
Cascaded Integrator Comb (CIC) LPF
F, 5300-Q
Cascaded Integrator Comb (CIC) LPF
keep 1 of N samples, configurable as a function of symbol rate
D, 5400-I
Decimate (↓ N)
D, 5400-Q
Decimate (↓ N)
Matched Filter, 5600, I
Matched Filter, 5600, Q
1900-I
1900-Q
Baseband Conversion, 4000
Filtering & Decimation, 5000

Fig. 5

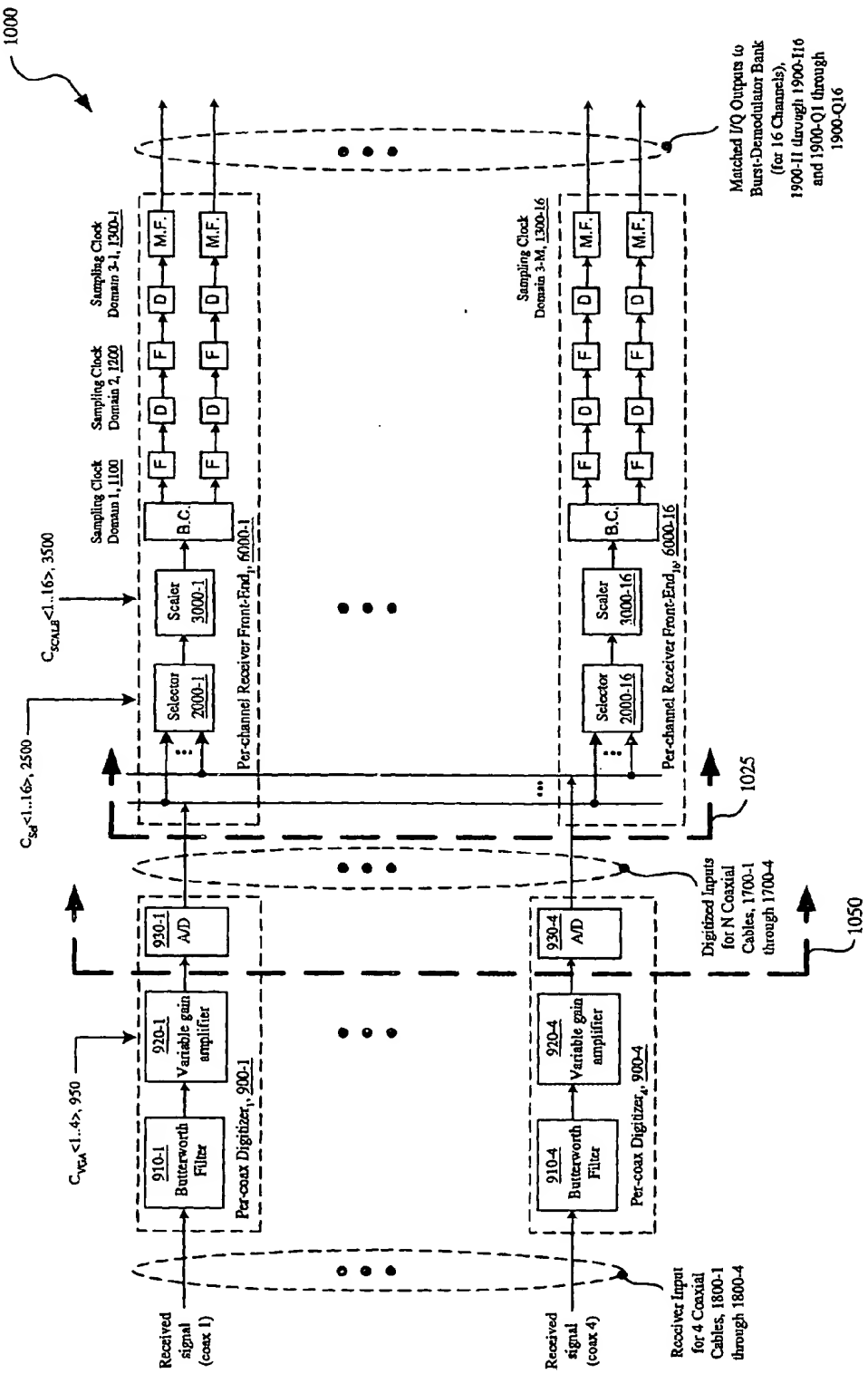

1000
Received signal (coax 1)
Received signal (coax 4)
Receiver Input for 4 Coaxial Cables, 1800-1 through 1800-4
910-1 Butterworth Filter
910-4 Butterworth Filter
920-1 Variable gain amplifier
920-4 Variable gain amplifier
930-1 A/D
930-4 A/D
Per-coax Digitizer1, 900-1
Per-coax Digitizer4, 900-4
Digitized Inputs for N Coaxial Cables, 1700-1 through 1700-4
1050
1025
Per-channel Receiver Front-End1, 6000-1
Per-channel Receiver Front-End16, 6000-16
Selector 2000-1
Selector 2000-16
Scaler 3000-1
Scaler 3000-16
B.C.
F
D
M.F.
Sampling Clock Domain 1, 1100
Sampling Clock Domain 2, 1200
Sampling Clock Domain 3-1, 1300-1
Sampling Clock Domain 3-M, 1300-16
Matched I/Q Outputs to Burst-Demodulator Bank (for 16 Channels), 1900-I1 through 1900-I16 and 1900-Q1 through 1900-Q16
C_{SCALE}<1..16>, 3500
C_{Sel}<1..16>, 2500
C_{VGA}<1..4>, 950

Fig. 6

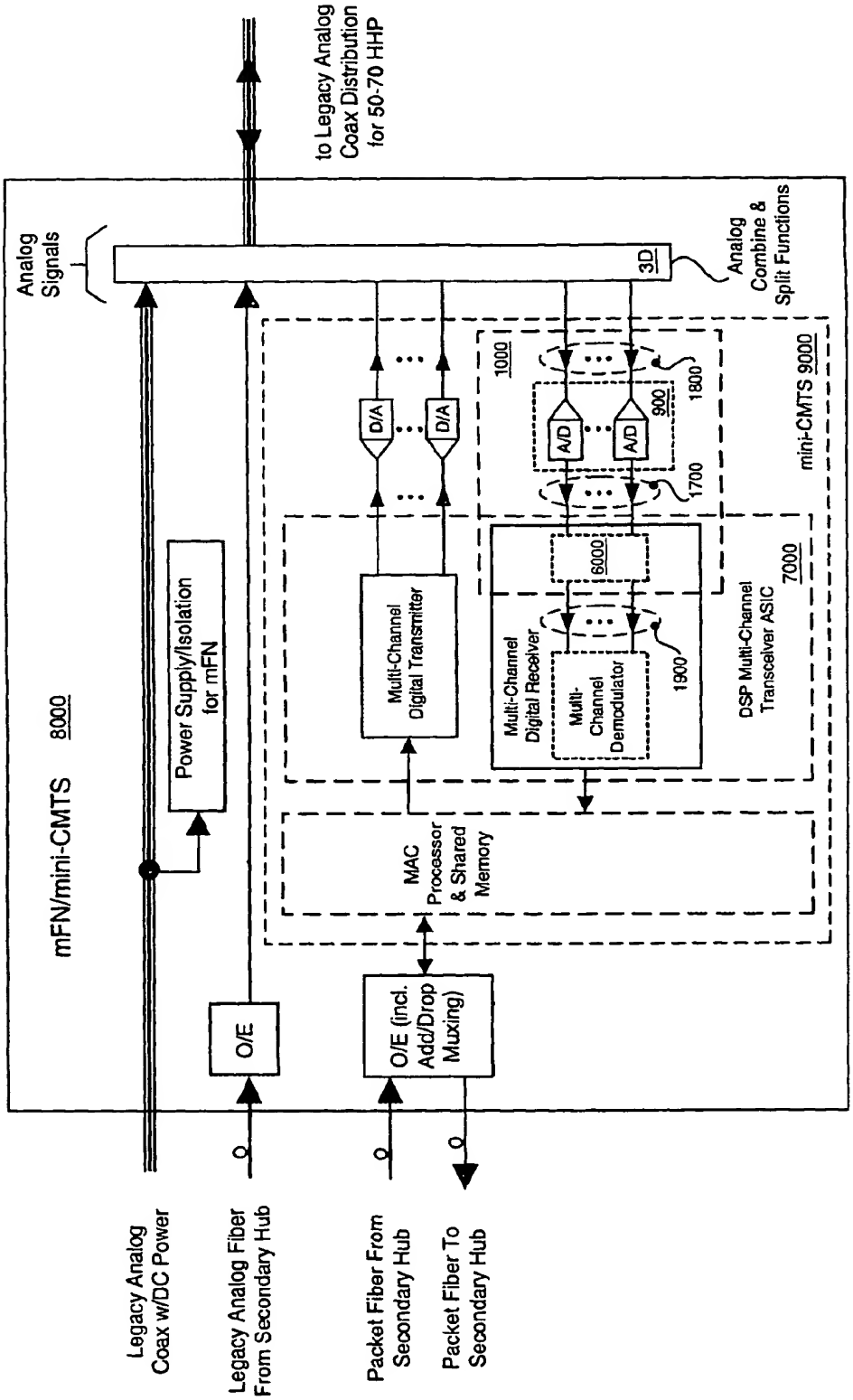

to Legacy Analog Coax Distribution for 50-70 HHP
Analog Signals
3D
Analog Combine & Split Functions
mini-CMTS 9000
1000
1800
900
A/D
A/D
1700
D/A
D/A
6000
Multi-Channel Digital Transmitter
Multi-Channel Digital Receiver
Multi-Channel Demodulator
1900
DSP Multi-Channel Transceiver ASIC
7000
MAC Processor & Shared Memory
Power Supply/Isolation for mFN
mFN/mini-CMTS 8000
O/E
O/E (incl. Add/Drop Muxing)
Legacy Analog Coax w/DC Power
Legacy Analog Fiber From Secondary Hub
Packet Fiber From Secondary Hub
Packet Fiber To Secondary Hub

Fig. 7

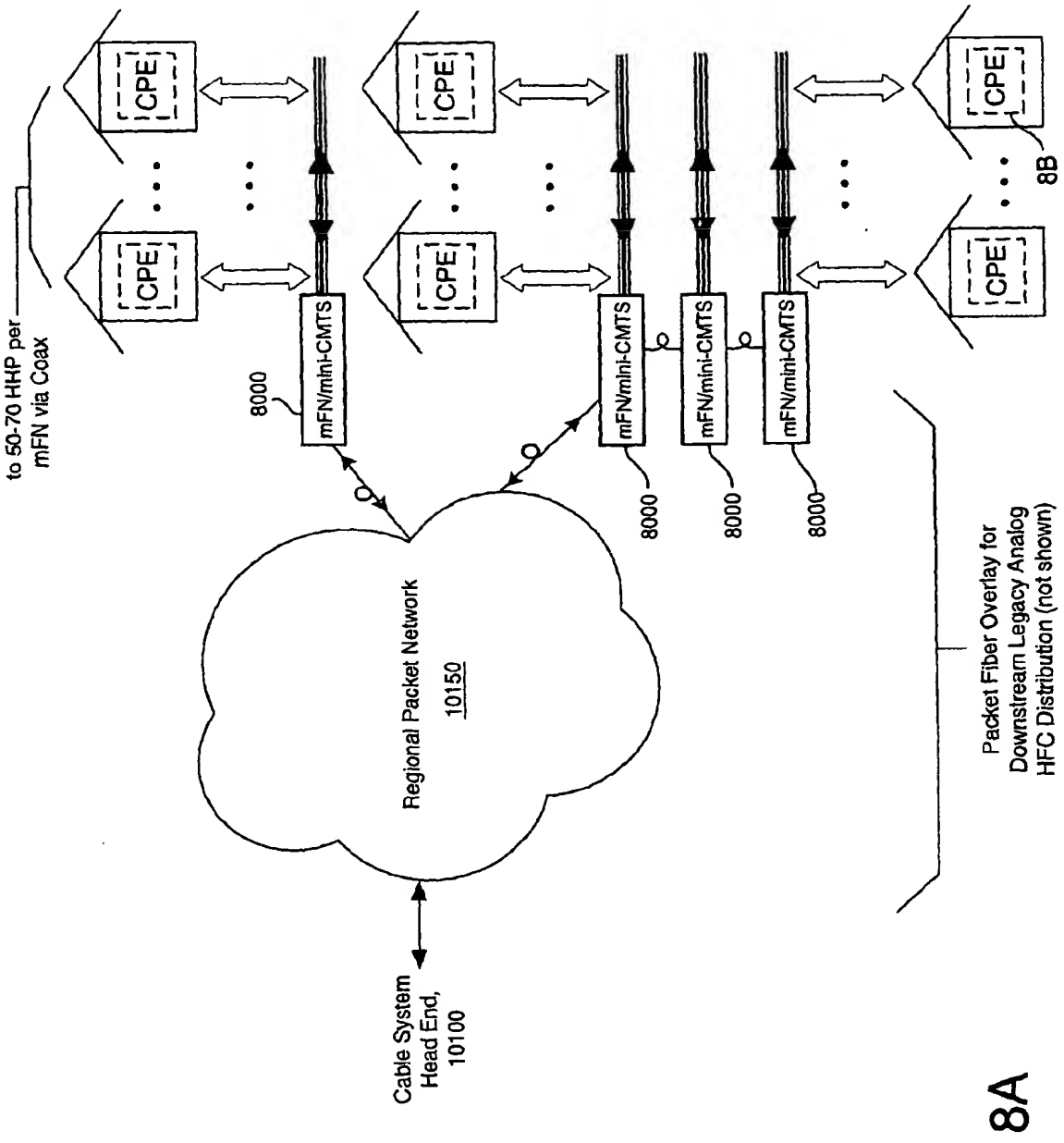
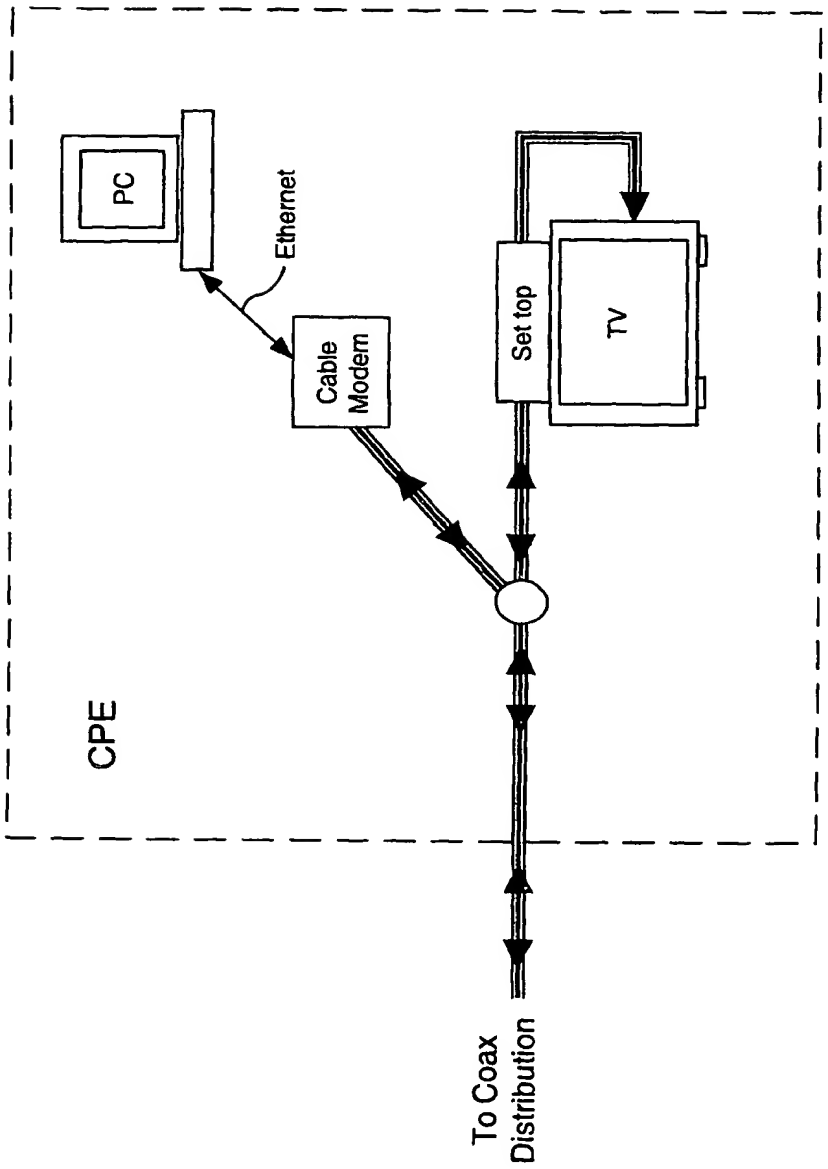

to 50-70 HHP per mFN via Coax
CPE
8000
mFN/mini-CMTS
8B
Regional Packet Network
10150
Cable System Head End, 10100
Packet Fiber Overlay for Downstream Legacy Analog HFC Distribution (not shown)

Fig. 8A



Prior Art
Fig. 8B

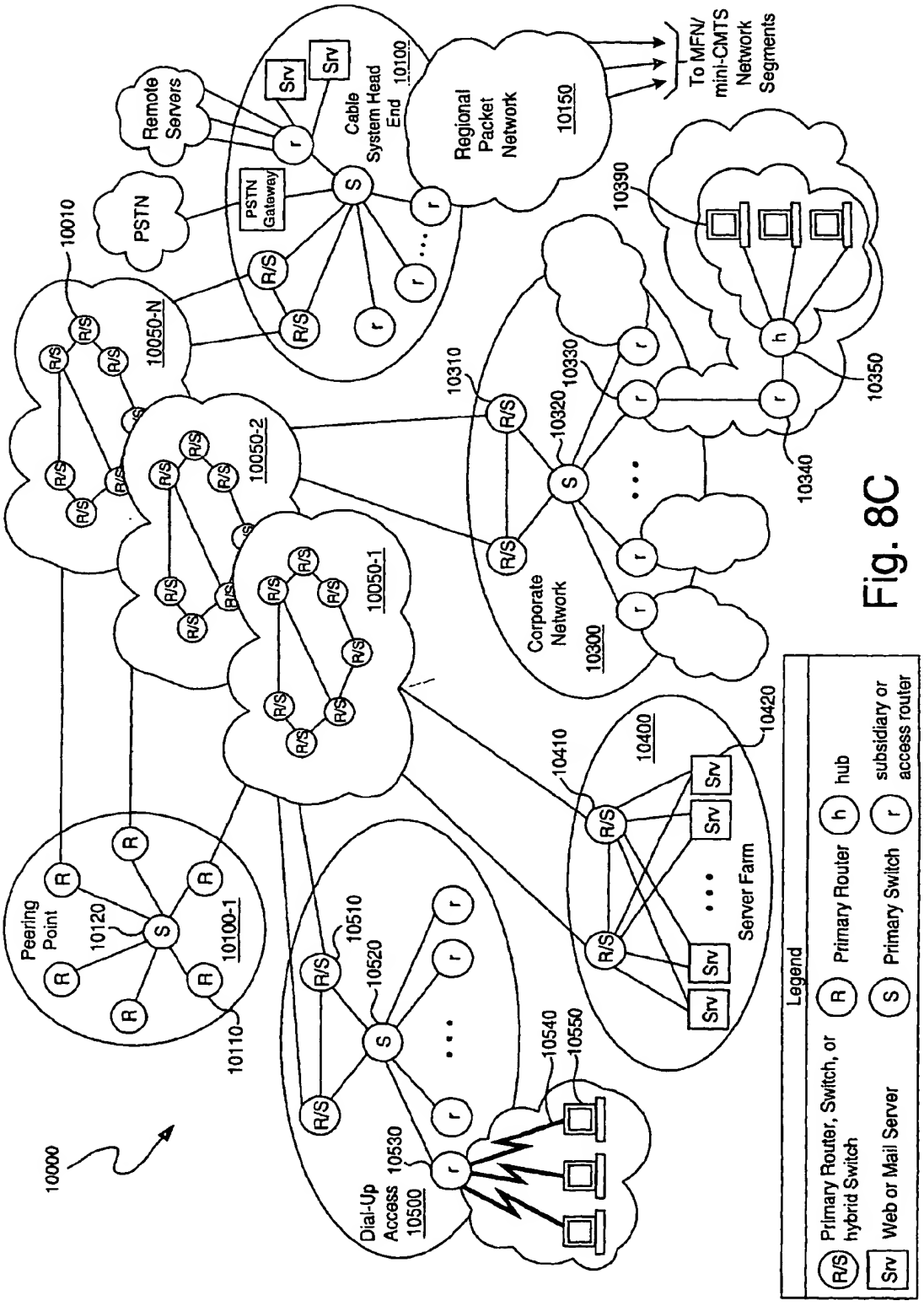

10000
Peering Point
10120
10100-1
10110
10010
10050-N
10050-2
10050-1
PSTN
Remote Servers
PSTN Gateway
Srv
Cable System Head End 10100
Regional Packet Network 10150
To MFN/ mini-CMTS Network Segments
10390
10350
10340
10310
10320
10330
Corporate Network 10300
10400
10410
10420
Server Farm
Dial-Up Access 10500
10510
10520
10530
10540
10550
Legend
Primary Router, Switch, or hybrid Switch
Primary Router
hub
Web or Mail Server
Primary Switch
subsidiary or access router

Fig. 8C

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 40 3506

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	US 5 454 007 A (DUTTA SANTANU) 26 September 1995 (1995-09-26) * abstract *	1,4	H03D3/00 H04N7/173
A	EP 0 809 403 A (AT & T CORP) 26 November 1997 (1997-11-26) * figure 4 *	1,4	
A	US 5 864 672 A (WOODWARD SHERYL LEIGH ET AL) 26 January 1999 (1999-01-26) * abstract *	1	
A	EP 0 841 817 A (AT & T CORP) 13 May 1998 (1998-05-13)		

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03B
H03D
H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 May 2001	Peeters, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
C : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 40 3506

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21-05-2001

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		CA 2219006 A	12-05-1998
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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82